

Endian Conventions for the AT91SC321RC

Introduction

“The nice thing about standards is that there are so many of them to choose from.”

Andres S. Tannenbaum

One of the more confusing standards in computer science is byte ordering and how it applies to specific devices and architectures. This application note is intended to clarify byte-ordering standards as they apply to the Atmel AT91SC321RC security chip.

Background

If memory were always accessed one byte at a time, there would be no confusion about byte ordering. However, in real systems we typically have different sized data that takes up more than one byte.

In general, the convention for byte ordering designates the labeling of memory locations with the *most significant byte* (MSB), the so-called “big end,” on the left. Architectures where the MSB is stored in memory location “0” are therefore referred to as *Big Endians*. Conversely, machines where the *least significant bit* (LSB) is stored in memory location “0” are called *Little Endians*.

Figures 1 and 2 consider a 32-bit word using 8-bit bytes:

Figure 1. Left-to-right Labels (Big Endian)

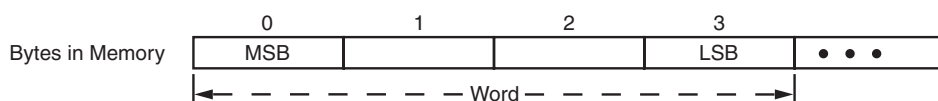
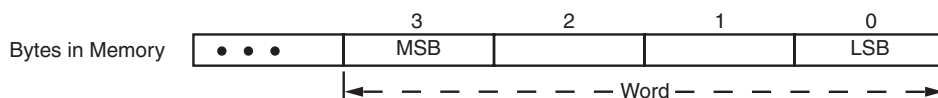


Figure 2. Right-to-left Labels (Little Endian)



In addition to byte ordering, the order of bits in each byte needs to be taken into consideration. In all configurations, the ordering of bytes is considered more important than the ordering of bits. Therefore, we classify architectures by the way they order bytes. When the byte and bit ordering differ, we use the term *inconsistent* to specify the subclassifications.

For example, if both the byte and bit ordering is left-to-right, it is designated *Consistent Big Endian*. The TI 9900 series is a good example of this architecture (see Figure 3).

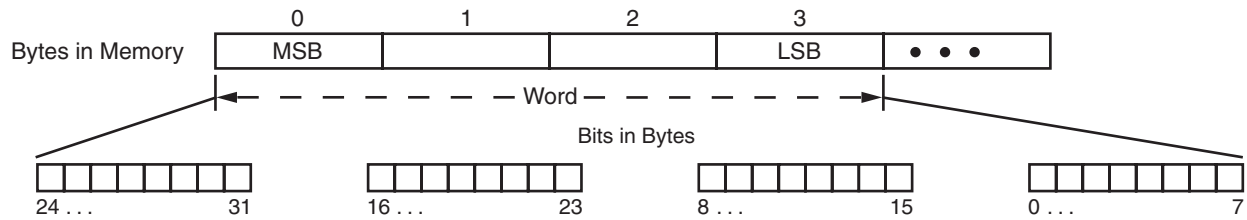


AT91SC321RC Byte Ordering

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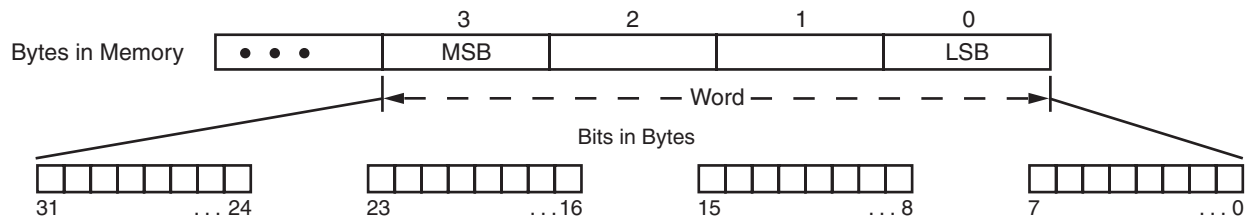


Figure 3. TI 9900 Series Architecture/Consistent Big Endian



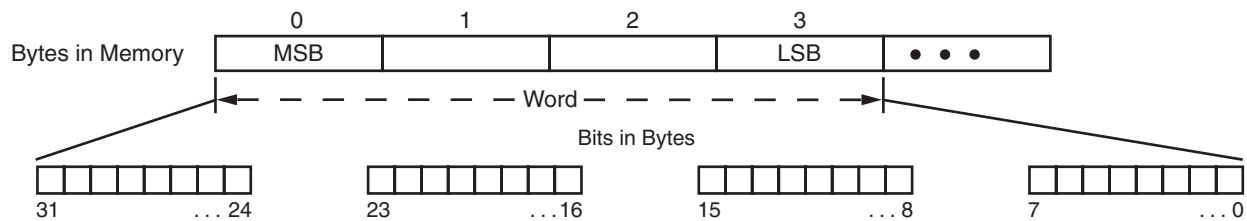
If byte and bit ordering are right-to-left, it is designated *Consistent Little Endian*. Intel® architectures use this format (see Figure 4).

Figure 4. Intel Architecture/Consistent Little Endian



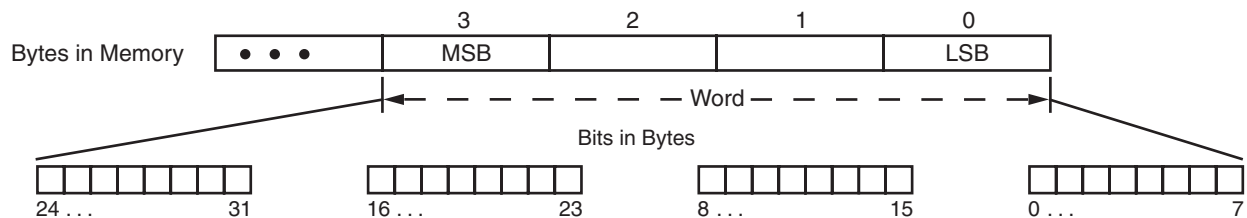
When byte ordering is left-to-right and bit ordering is right-to-left, it is called *Inconsistent Big Endian*. The most commonly used format is in the Motorola 68000 series machines (see Figure 5).

Figure 5. Motorola 68000 Architecture/Inconsistent Big Endian



Finally, when byte ordering is right-to-left and bit ordering left-to-right, it is designated *Inconsistent Little Endian*. This type of architecture is not currently in use (see Figure 6).

Figure 6. Inconsistent Little Endian



AT91SC321RC Byte Ordering Information

The AT91SC321RC internal architecture supports Consistent Little Endian byte alignment only.



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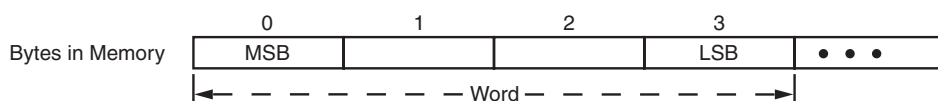
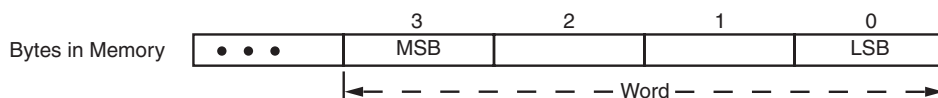


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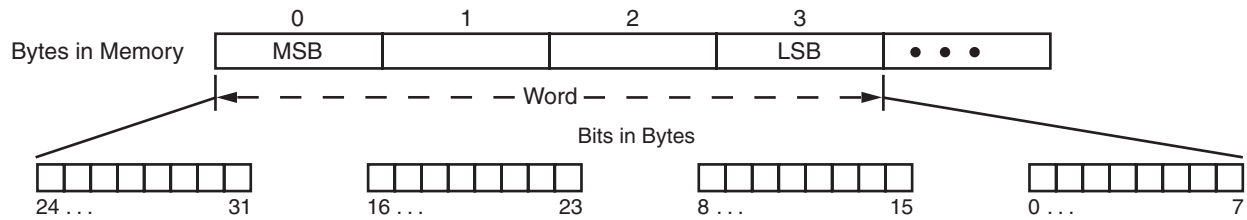


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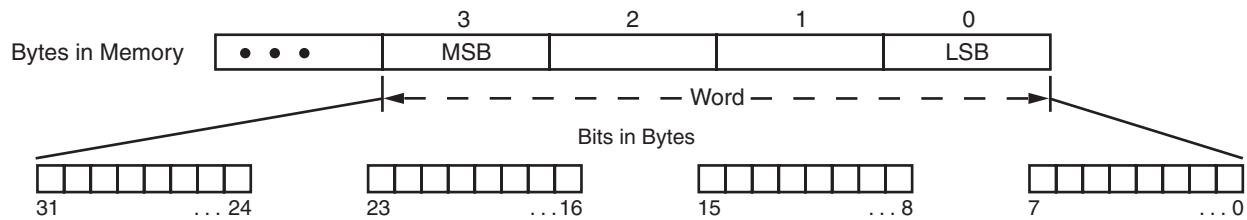


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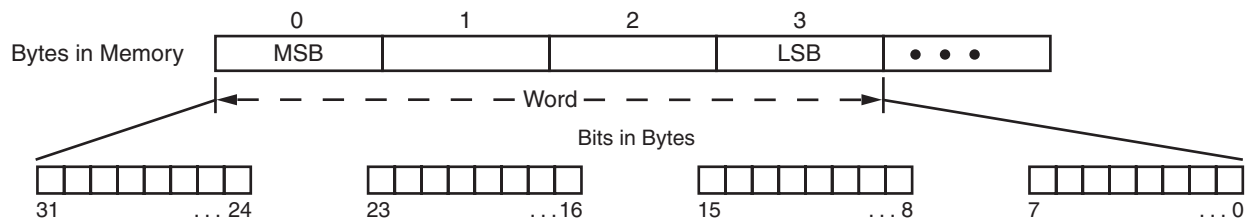
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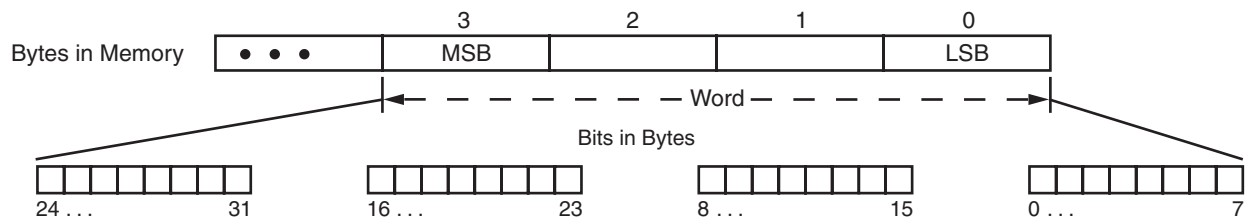
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